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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. Yo999-153DIV

In Re Application Of: Chen, et al.

Serial No.	Filing Date	Examiner	Group Art Unit
09/748,256	12/27/2000	Nadav, Ori	2811

Invention: Method for Fabricating Complementary Metal Oxide Semiconductor (CMOS) Devices on a Mixed Bulk and Silicon-On-Insulator (SOI) Substrate

TO THE COMMISSIONER FOR PATENTS:

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Signature

Dated: 4/19/04

Phillip E. Miller
Registration No. 46,060
McGinn & Gibb, PLLC
8321 Old Courthouse Road
Suite 200
Vienna, VA 22182-3817

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Chen, et al.

Serial No.: 09/748,256 **Group Art Unit:** 2811

Filed: December 27, 2000 **Examiner:** Ori Nadav

For: METHOD FOR FABRICATING COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS) DEVICES ON A MIXED BULK AND SILICON-ON-INSULATOR (SOI) SUBSTRATE

Honorable Commissioner of Patents
Alexandria, VA 22313-1450

APPELLANT'S BRIEF ON APPEAL

Sir:

Appellant respectfully appeals the final rejection of claims 29-39 and 41-57 in the Office Action dated November 19, 2003. A Notice of Appeal was filed herein on February 19, 2004.

I. REAL PARTY IN INTEREST

The real party in interest for this appeal and the present application is International Business Machines Corporation by way of an Assignment recorded in the U.S. Patent and Trademark Office at Reel 010029, Frame 0423.

II. RELATED APPEALS AND INTERFERENCES

There are presently no appeals or interferences, known to the Appellants, the Appellants'

representatives or the Assignees, which will directly affect or be directly affected by or have a bearing upon the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 29-39 and 41-57 are all the claims presently pending in the application, and are fully set forth in the attached Appendix.

Claims 29-36, 41-42 and 45-57 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sun (U.S. Patent No. 5,399,507). Claims 37-39 and 43-44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sun, in further view of Tanaka (JP Patent No. 10-303385).

Appellant respectfully appeals these rejections.

IV. STATUS OF AFTER-FINAL AMENDMENTS

An after-final Amendment was filed on January 21, 2004. By an Advisory Action mailed February 13, 2004, the Examiner indicated that the Amendment would not be entered.

However, Appellant notes that the claim amendments included therein clearly do not raise new issues and serve to clarify the issues on appeal. For example, in the Amendment, claims 29, 41, 45-46 were amended to include a portion of a limitation from claim 57. Therefore, this Amendment should have been entered by the Examiner.

Therefore, Appellant files concurrently herewith a second after-final Amendment which is substantially identical to the Amendment filed on January 21, 2004. Appellant respectfully

requests that the Examiner enter this second after-final Amendment.

Appellant notes that the claims are set forth in the attached Appendix presuming entry of the second after-final Amendment which is filed concurrently herewith.

V. SUMMARY OF INVENTION

Appellant's invention (e.g., as recited in claim 29) is directed to a semiconductor device including a bulk silicon region comprising single crystal silicon, and a silicon-on-insulator (SOI) region which includes an insulator layer which is formed beneath an upper portion of the single crystal silicon and has at least one lateral end portion adjacent to a lower portion of the single crystal silicon, and at least one isolation oxide formed in the upper portion of the single crystal silicon so as to form at least one island of the single crystal silicon on an upper surface of the insulator layer.

Importantly, the at least one isolation oxide includes a first isolation oxide formed adjacent to a first end portion of the insulator layer, a second isolation oxide formed adjacent to a second end portion of the insulator layer and a third isolation oxide formed on a middle portion of the insulator layer, the first and second isolation oxides extending laterally beyond the first and second end portions, respectively.

Conventional substrates having an SOI region are formed either by separation by implantation of oxygen (SIMOX) or by a cladding process where an oxide layer is formed in a first surface of a first substrate, a second substrate is bonded to the first surface, and elements are then formed in the second substrate. However, such conventional devices do not include a first

isolation oxide formed adjacent to a first end portion of the insulator layer, a second isolation oxide formed adjacent to a second end portion of the insulator layer and a third isolation oxide formed on a middle portion of the insulator layer, the first and second isolation oxides extending laterally beyond the first and second end portions, respectively.

Appellant's invention, on the other hand, includes a first isolation oxide formed adjacent to a first end portion of the insulator layer, a second isolation oxide formed adjacent to a second end portion of the insulator layer and a third isolation oxide formed on a middle portion of the insulator layer, the first and second isolation oxides extending laterally beyond the first and second end portions, respectively (Application at Figure 1C-1D; page 7, line 7-page 8, line 11).

In Appellant's invention, the upper portion of silicon overlying the insulator layer may be formed over the insulator layer by depositing amorphous silicon on the insulator layer and the lower portion of the single crystal silicon, and crystallizing the amorphous silicon by using the lower portion of the single crystal silicon as a crystal growth seed (Application at page 7, lines 17-21). As a result, non-ideal silicon may exist "on the seam where the crystallization of the epitaxial silicon from both edges meet" (Application at page 10, lines 7-12; Figure 1D). Thus, by including an isolation oxide on a middle portion of the insulator layer, this "non-ideal" portion of the silicon may be removed from the substrate (Application at page 10, lines 13-20).

VI. ISSUES PRESENTED FOR REVIEW

The issues presented for review by the Board of Patent Appeals and Interferences include whether claims 29-36, 41-42 and 45-57 are not patentable under 35 U.S.C. § 103(a) over Sun

(U.S. Patent No. 5,399,507) (hereinafter "Sun"), and whether claims 37-39 and 43-44 are not patentable under 35 U.S.C. § 103(a) over Sun, in further view of Tanaka (JP Patent No. 10-303385)(hereinafter "Tanaka"), as alleged by the Examiner.

VII. GROUPING OF THE CLAIMS

As supported by the following arguments, dependent claims 30-39 and 50-57 are patentably distinct from independent claim 29.

Each dependent claim 30-39 and 50-57 (which depend either directly or indirectly from claim 1) recites additional features, not defined in the respective independent claim. As discussed in greater detail below, the features defined by these dependent claims are not merely illustrations or examples, but patentable features which prevent the dependent claims from standing or falling with independent claim 29.

In addition, independent claims 41, 45 and 46 are patentably distinct from each other, and patentably distinct from independent claim 29 and claims 30-39 and 50-57 which depend (directly or indirectly) from claim 29. Further, dependent claims 42-44 are patentably distinct from independent claim 41 from which they depend (directly or indirectly), and dependent claims 47-49 are patentably distinct from claim 46 from which they depend.

VIII. ARGUMENT

A. The Examiner's Position

As set forth on pages 2-3 of the Office Action dated November 19, 2003, the Examiner

rejected claims 29-36, 41-42 and 45-57 under 35 U. S. C. §103(a) as allegedly unpatentable over Sun, stating:

"Claims 29-26, 41-42 and 45-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun (5,399,507).

Regarding claims 29, 36, 41, 45 and 46, Sun teaches in Figure 4 and related text a hybrid semiconductor device comprising a bulk silicon region 11 comprising single crystal silicon (column 2, lines 61-62) and an SOI region comprising an insulator layer 18 formed beneath an upper portion of the single crystal silicon and has at least one lateral end portion adjacent to a lower portion of the single crystal silicon, and at least two isolation oxides 22, 24 formed in an upper portion of the single crystal silicon so as to form a plurality of islands of the single crystal silicon on an upper surface of the insulator layer, wherein a sidewall of the insulator layer 23 is angled so that a width of the upper surface of the insulator layer is larger than a width of a lower surface of the insulator layer, wherein at least one isolation oxide comprises a first isolation oxide 24 formed adjacent to a first end portion of the insulator layer, a third isolation oxide 22 formed adjacent to a middle portion of the insulator layer, and wherein the first isolation oxide extends laterally beyond the first end portion.

Sun does not teach a second isolation oxide formed adjacent to a second end portion of the insulator layer wherein the second isolation oxide extends laterally beyond the second end portion.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a second isolation oxide formed adjacent to a second end portion of the insulator layer wherein the second isolation oxide extends laterally beyond the second end portion in Sun's device in order to form the device as taught by Sun by providing protection to the thin film active area also at the second end portion of the device. The combination is motivated by the teachings of Sun who points out the dual function of the isolation oxide which is formed adjacent to an end portion of the insulator layer (column 3, lines 34-48)." *(Office Action at pages 2-3).*

Appellant notes that nowhere in the Office Action does the Examiner specifically address the limitations included in claim 57.

With respect to claims 37-39 and 43-44, the Examiner concedes that Sun does not teach or suggest "*forming a DRAM memory device on the silicon bulk and a MOSFET logic device on the SOI region*". However, the Examiner alleges that this feature is taught by Tanaka and that Tanaka would have been combined with Sun to form the invention of claims 37-39 and 43-44.

Appellant also notes that in the Advisory Action dated February 13, 2004, the Examiner refused to enter the Amendment filed on January 21, 2004, alleging that "the new limitations of a third isolation oxide formed on a middle portion of said insulator layer, as recited in claims 29, 41, 45 and 46, warrant further consideration and/or search" (Advisory Action at page 2).

B. Appellant's Position

1. Claim Construction

Appellant respectfully submits that the claims are clearly written, unambiguous and subject to little interpretation. Specifically, Appellant submits that the claims recite terms which are generally accepted in the art.

Further, it is well-settled that claims would likely be construed in light of the written specification. See, e.g., Uniroyal, Inc. v. Rudkin-Wiley Corp., 5 U.S.P.Q.2d 1434, 1441 (Fed. Cir. 1988). Further, in determining the scope of claim limitations, words in a claim are given their ordinary and accustomed meaning unless it appears that the inventor used them differently. Envirotech Corp. v. Al George, Inc., 730 F.2d 753, 221 U.S.P.Q. 473 (Fed. Cir. 1984) at 477.

Appellant respectfully submits that there, absent some indication in the specification that would require the terms recited in the claims to be given a special meaning, the terms should be given their ordinary and accustomed meaning, as they are understood by one of ordinary skill in the art.

Further, Appellant submits that the inventive semiconductor device (e.g., substrate, hybrid bulk silicon and silicon-on-insulator (SOI) substrate) is clearly described by the specification. For example, the Application states that one exemplary embodiment of the invention includes "at least one isolation oxide".

Appellant submits that the term "isolation oxide" is clear and unambiguous. The term "isolation" may be defined as "an act or instance of isolating", and the term "oxide" may be defined as "a compound in which oxygen is bonded to one or more electropositive atoms"

(*Webster's New Universal Unabridged Dictionary,* 1996, pages 1013, 1383). Further, the term is commonly construed by those of ordinary skill in the art to mean an oxide which is used to isolate regions of a semiconductor device or substrate. Thus, Appellant submits that the term "isolation oxide" would likely be construed by one of ordinary skill in the art to mean a compound in which oxygen is bonded to one or more electropositive atoms and which is isolating (e.g., isolates regions of a semiconductor device or substrate).

Appellant further submits that the terms "adjacent to", "end portion", "middle portion", and "on" are clear and unambiguous. For example, the term "adjacent" may be defined as "near or close (to something); adjoining", the term "end" may be defined as "the part at, toward, or near either of the extremities of anything; tip", the term "middle" may be defined as "halfway between two given points, times, limits, etc.", the term "portion" may be defined as "a part or limited quantity of anything" (*Webster's New World Dictionary, Third College Edition,* 1988, pages 16, 448, 858 and 1052). Further, Appellant submits that the term "on" is commonly construed by those of ordinary skill in the art to mean "in a position above".

Therefore, Appellant respectfully submits that the claims are clearly defined and unambiguous. Specifically, Appellant submits that the limitation "*wherein said at least one isolation oxide comprises a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first and second end portions, respectively*" which is included in claims 29, 41 and 45-46 is clear and unambiguous.

Thus, Appellant submits that the claims and written specification are clear and unambiguous and subject to little interpretation. Specifically, it is clear that the specification explains in detail the elements of the claims.

2. The Prior Art Rejections

a. Independent Claims 29, 41 and 45-46: Comparison of claims 29, 41 and 45-46 to the Sun Reference

Claim 29 recites as follows:

"*A semiconductor device comprising:*

a bulk silicon region comprising single crystal silicon; and

a silicon-on-insulator (SOI) region comprising:

an insulator layer which is formed beneath an upper portion of said single crystal silicon and has at least one lateral end portion adjacent to a lower portion of said single crystal silicon; and

at least one isolation oxide formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer,

wherein said at least one isolation oxide comprises a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and

second isolation oxides extending laterally beyond said first and second end portions, respectively."

Therefore, as noted above, the claimed invention as recited in claim 29 includes a semiconductor device which is not taught or suggested by the Sun. For example, in the claimed semiconductor device, the at least one isolation oxide includes a first isolation oxide formed adjacent to a first end portion of the insulator layer, a second isolation oxide formed adjacent to a second end portion of the insulator layer and a third isolation oxide formed on a middle portion of the insulator layer, the first and second isolation oxides extending laterally beyond the first and second end portions, respectively.

Appellant respectfully submits that these features are not taught or suggested by the Sun reference cited by the Examiner.

i. The Rejection is Erroneous as a Matter of Law

The Examiner's rejection is erroneous as a matter of law.

Specifically, 35 U. S. C. §103(a) states:

"[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the

invention was made".

Generally, there are several well known statements on the requirements of establishing obviousness. For example, it has been stated that the factual inquiries which must precede a legal conclusion on obviousness are the determination of the scope and content of the prior art, the differences between the claimed invention and the prior art, the level of ordinary skill in the art, and objective evidence of nonobviousness, such as commercial success, long-felt but unsolved needs which the invention has satisfied, failure of others to make the claimed invention, copying of the alleged invention, and unexpected results brought about by the invention. DMI, Inc. vs. Deere & Col., 231 U. S. P. Q. 276 (Fed. Cir. 1986).

It has been further stated that "[t]he consistent criterion for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this process should be carried out and would have a reasonable likelihood of success, viewed in the light of the prior art" In re Dow Chem. Co., 837 F.2d 469, 473 (Fed. Cir. 1988).

Clearly, the Examiner has failed to show that each and every element as set forth in claim 29 is taught or suggested by the Sun reference. For example, the Examiner has failed to show that Sun teaches or suggests *"wherein said at least one isolation oxide comprises a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first and second end portions, respectively."* as recited in claim 29.

In view of all of the foregoing, Appellant respectfully submits that the Examiner's rejection is erroneous as a matter of law. Thus, the Board is respectfully requested to remove this rejection of claim 29.

ii. The Rejection is Erroneous as a Matter of Fact

Further, the Examiner's rejection is erroneous as a matter of fact.

The Examiner alleges that Sun makes obvious the claimed invention of claims 29-36, 41-42 and 45-57. Appellant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Sun.

Sun discloses a mixed thin-film and bulk semiconductor substrate (10, 30) for integrated circuit applications is made with two different processes. In the first process, a standard wafer (11) is masked around its periphery (14). The internal unmasked portion (16) is implanted with an insulating species to form a buried dielectric layer (18), thus forming a mixed thin-film and bulk semiconductor substrate. Alternatively, a thin-film wafer may be masked on an internal portion (36) and then etched to expose a portion (40) of the underlying bulk substrate (11') around the periphery of the wafer. An epitaxial layer (50) is then grown to build up the exposed bulk portion to form the mixed substrate. An isolation region (24, 52, 46, 54) is formed at a boundary between the thin-film portion and the bulk portion. Devices (27, 28, 28') having different voltage requirements may then be formed overlying appropriate portions of the mixed substrate.

However, Sun does not teach or suggest "*wherein said at least one isolation oxide*

comprises a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first and second end portions, respectively", as recited in claims 29, 41 and 45-46.

As noted above, unlike conventional substrates having an SOI region which are formed either by separation by implantation of oxygen (SIMOX) or by a cladding process, in the claimed invention, the upper portion of silicon overlying the insulator layer may be formed over the insulator layer by depositing amorphous silicon on the insulator layer and the lower portion of the single crystal silicon, and crystallizing the amorphous silicon by using the lower portion of the single crystal silicon as a crystal growth seed (Application at page 7, lines 17-21). However, in this case, non-ideal silicon may exist "on the seam where the crystallization of the epitaxial silicon from both edges meet" (Application at page 10, lines 7-12; Figure 1D). Thus, by forming an isolation oxide on a middle portion of the insulator layer, this "non-ideal" portion may be removed from the substrate (Application at page 10, lines 13-20).

As a result, the claimed invention includes a first isolation oxide formed adjacent to a first end portion of the insulator layer, a second isolation oxide formed adjacent to a second end portion of the insulator layer and a third isolation oxide formed on a middle portion of the insulator layer, the first and second isolation oxides extending laterally beyond the first and second end portions, respectively (Application at Figure 1C-1D; page 7, line 7-page 8, line 11). This feature is not taught of suggested by conventional substrates.

Clearly, this feature is not taught or suggested by Sun. Indeed, as noted above, the Examiner has completely neglected to address this limitation in the Office Action dated November 19, 2003. Specifically, Appellant notes that a portion of the above-referenced limitation (e.g., a third isolation oxide formed on a middle portion of the insulator layer) was previously included in claim 57 of the present Application and was incorporated into claims 29, 41 and 45-46 by the Amendment dated January 21, 2004. However, nowhere in the Office Action or in the Advisory Action dated February 13, 2004 does the Examiner address the limitations of claim 57.

Further, the Examiner attempts to equate the isolation region 22 in Sun, with the isolation oxide formed near a "middle portion" of the insulator layer in the claimed invention. However, Figure 4 clearly does not show the isolation region 22 formed in the middle of the "buried dielectric layer" 18. Indeed, Figure 4 (as with the other drawings) cuts off the substrate 11, so it is impossible determine at what portion of the dielectric layer 18 the isolation region 22 is formed.

In fact, nowhere does Sun teach or suggest forming the region 22 "on the middle portion" of the buried dielectric 18. Instead, Sun merely states that "[i]solation region 22 is formed solely in the thin-film portion 20 of the substrate10" (Sun at col. 3, lines 28-29). Appellant points out that this could be many places other than "on the middle portion". For example, this could be satisfied by forming the isolation region near the left edge of the dielectric layer 18, or near the right edge of the dielectric layer 18.

Moreover, Sun would have no reason to form the isolation region 22 on the middle

portion of the buried dielectric 18. Indeed, the quality of the silicon above the dielectric 18 is the same over the length of the dielectric 18. Therefore, it would in no way benefit the Sun device to form the isolation region 22 in the middle of the dielectric. Thus, there would be no reason to modify the Sun device to include this feature.

Further, Sun is directed to a standard separation by implantation of oxygen (e.g., SIMOX) process. The Application specifically states that claimed invention may be used to replace the conventional SIMOX technique and provides numerous benefits and advantages over the conventional SIMOX technique (Application at page 5, lines 2-10)

As explained in the Application, the conventional SIMOX technique results in the silicon exposed to such implantation of oxygen having a large number of defects (in fact, this is one of the problems which the claimed invention is intended to address). Thus, the silicon regions above the dielectric layer 18 in Sun would contain a large amount of defects.

The claimed invention, on the other hand, does not include such defects scattered all over the upper portion of the silicon substrate. Indeed, in the claimed invention, any defective portions may be localized (e.g., near a middle portion of the insulator layer) and can, therefore, be easily replaced with an isolation oxide.

As noted above, these advantages of the claimed invention over a substrate subjected to a SIMOX process is clearly set forth in the Application. However, the Examiner somehow surprisingly refuses to recognize these benefits.

For example, the Examiner states in the Office Action that Sun does not teach that the silicon above the dielectric layer includes a defective region "in absence of evidence to the

contrary" he considers the silicon islands to be substantially devoid of defects. **Appellant would respectfully point out that the specification** states:

> "*as compared to the conventional patterned SIMOX technique, which results in a much higher number of defect counts per unit area (or defect density), the method of the present invention results in a much better substrate quality. This higher substrate quality is because the stress from lattice mismatch (e.g., of the oxide and the silicon) is more by high energy oxygen implantation. The defective regions resulting from the method of the present invention are also predictable and therefore can be completely removed in a subsequent shallow trench formation*" (Application at page 5, lines 2-10).

Thus, Appellant respectfully submits that there is plenty of evidence in the record establishing that the silicon above the dielectric layer in the Sun device includes a high number of defect counts per unit area. Indeed, this fact is very well known to any person of ordinary skill in this art. In fact, this is the only evidence in this case regarding the quality of the silicon above the dielectric layer. That is, there is no evidence in the case that would contradict the Application. Therefore, Appellant respectfully submits that the Examiner, having failed to provide any evidence to the contrary to support his tenuous position, is bound by this evidence.

Further, with respect to claim 4, the Examiner states that it would obvious to modify Sun to include an angled sidewall of the insulator layer. However, Appellant would point out that it is impossible to form an angled sidewall using a SIMOX process as in Sun. Therefore, the Examiner is clearly incorrect.

In view of all of the foregoing, Appellant respectfully submits that the Examiner's rejection is erroneous as a matter of fact. Thus, the Board is respectfully requested to remove this rejection of claims 29, 41 and 45-46.

b. Dependent Claims 30-35, 42 and 47-57: Comparison of Dependent Claims 30-35, 42 and 47-57 with the Sun Reference

While independent claims 29, 41 and 45-46 are directed to statutory subject matter, as discussed above, claims 30-35, 42 and 47-57 which each depend from one of claims 29, 41 and 45-46, define similar statutory subject matter separately and distinctly from the independent claims as these dependent claims recite additional elements clearly providing useful, concrete and tangible results.

Claim 30 depends from claim 29, and recites "*wherein said at least one island of single crystal silicon comprises a plurality of islands and said at least one isolation oxide comprises a plurality of isolation oxides, and each of said islands are interspaced between said isolation oxides to form a shallow trench isolation (STI) structure*" (Application at Figure 1D).

Claim 31 depends from claim 30, and recites *"wherein said insulator layer has a thickness in a range of 1000Å and 5000Å*"(Application at page 7, lines 14-15).

Claim 32 depends from claim 29, and recites "*wherein said upper portion of said single crystal silicon is formed over said insulator layer by depositing amorphous silicon on said insulator layer and said lower portion of said single crystal silicon, and crystallizing said amorphous silicon by using said lower portion of said single crystal silicon as a crystal growth*

seed"(Application at page 7, line 7-page 8, line 11).

Claim 33 depends from claim 32, and recites *"wherein said isolation oxides are formed in defective portions of said single crystal silicon*"(Application at page 7, line 7-page 8, line 11).

Claim 34 depends from claim 31, and recites *"wherein said isolation oxides and said insulator layer are formed of a same material*"(Application at page 7, line 7-page 8, line 11).

Claim 35 depends from claim 29, and recites *"wherein an upper surface of said isolation oxides and said single crystal silicon are planarized*"(Application at page 7, line 7-page 8, line 11).

Claim 42 depends from claim 41, and recites "*wherein said insulator layer is formed in an SOI region of said substrate and not in a bulk silicon region of said substrate* (Application at page 7, line 7-page 8, line 11).

Claim 47 depends from claim 46, and recites *"wherein said upper portion of said single crystal silicon substrate is formed on said insulator layer by growing said single crystal silicon substrate horizontally over said insulator layer*"(Application at page 7, line 7-page 8, line 11).

Claim 48 depends from claim 46, and recites "*wherein said upper portion of said single crystal silicon is formed by depositing amorphous silicon on said insulator layer and said lower portion of said single crystal silicon substrate, annealing said amorphous silicon so that, using said lower portion of said single crystal silicon substrate as a crystal growth seed, said amorphous silicon is converted to single crystal silicon having a same orientation as said lower portion of said single crystal silicon substrate*"(Application at page 7, line 7-page 8, line 11).

Claim 49 depends from claim 48, and recites "*wherein said isolation oxides are formed*

by forming isolation trenches in defective portions of said upper portion of said single crystal silicon, and depositing oxide in said isolation trenches (Application at page 8, line 21).

Claim 50 depends from claim 29, and recites "*wherein an angle between a bottom surface of said insulator layer and a sidewall of said insulator layer is about 103 °*"(Application at page 8, line 21).

Claim 51 depends from claim 29, and recites "*wherein a crystal orientation and structure of said upper portion of said single crystal silicon follows a crystal orientation and structure of said lower portion of said single crystal silicon*"(Application at page 6, line 17-page 16, line 5).

Claim 52 depends from claim 29, and recites "*wherein said upper portion of said single crystal silicon comprises crystallized amorphous silicon*"(Application at page 10, lines 7-12).

Claim 53 depends from claim 29, and recites "*wherein said insulator layer has a width in a range of about 2 μm to 10 μm*"(Application at page 7, lines 15-16).

Claim 54 depends from claim 29, and recites "*wherein said upper portion of said single crystal silicon has a thickness in a range of about 500 Å to 3000 Å*"(Application at page 9, lines 10-11).

Claim 55 depends from claim 30, and recites "*wherein said plurality of islands of single crystal silicon are wholly formed on said insulator layer*"(Application at Figure 1D).

Claim 56 depends from claim 29, and recites "*wherein said at least one island of single silicon crystal is substantially devoid of a defective region*"(Application at page15, lines 10-19).

Claim 57 depends from claim 29, and recites "*wherein said first and second isolation*

oxides are formed at least partially on said first and second end portions, respectively" (Application at Figure 1D).

Therefore, the dependent claims 30-35, 42 and 47-57 define elements and limitations which further place the claimed invention squarely in the realm of statutory subject matter and which provide a useful, tangible and concrete result.

Therefore, dependent claims 30-35, 42 and 47-57, like independent claims 29, 41 and 45-46, include at least one element which is not taught or suggested by the cited references, or any combination of the cited references.

c. Dependent Claims 37-39 and 43-44: Comparison of Dependent Claims 37-39 and 43-44 with the Sun Reference and the Tanaka Reference

The Examiner alleges that Tanaka would have been combined with Sun to form the claimed invention of claims 37-39 and 43-44. Appellant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Tanaka discloses a method of integrally forming a high-performance hybrid element. In the method, a silicon substrate 3 is exposed by selectively removing a silicon layer 1 and an insulating layer 2 from a silicon-on-insulator(SOI) substrate, and desired semiconductor elements 11 are respectively formed on the exposed silicon substrate 3 and the silicon layer 1 (Tanaka at Abstract).

However, Appellant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions.

Specifically, Sun is directed to a method of forming a thin film and bulk semiconductor substrate using SIMOX, whereas Tanaka is directed to a method of forming a DRAM device. Therefore, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Further, Appellant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, contrary to the Examiner's allegations, neither of these references teach or suggest their combination. Therefore, Appellant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, neither Sun, nor Tanaka, nor any combination thereof teaches or suggests "*wherein said at least one isolation oxide comprises a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first and second end portions, respectively*", as recited in claims 29, 41 and 45-46.

As noted above, unlike conventional substrates having an SOI region which are formed either by separation by implantation of oxygen (SIMOX) or by a cladding process, in the claimed

invention, the upper portion of silicon overlying the insulator layer may be formed over the insulator layer by depositing amorphous silicon on the insulator layer and the lower portion of the single crystal silicon, and crystallizing the amorphous silicon by using the lower portion of the single crystal silicon as a crystal growth seed (Application at page 7, lines 17-21). However, in this case, non-ideal silicon may exist "on the seam where the crystallization of the epitaxial silicon from both edges meet" (Application at page 10, lines 7-12; Figure 1D). Thus, by forming an isolation oxide on a middle portion of the insulator layer, this "non-ideal" portion may be removed from the substrate (Application at page 10, lines 13-20).

Clearly, Tanaka does not teach or suggest these novel features. Indeed, the Examiner does not even rely on Tanaka as disclosing this feature, but only relies on Tanaka as allegedly disclosing a memory device formed in the bulk silicon region and a logic device formed in the SOI region.

In fact, Tanaka merely discloses that a logic circuit 13 is formed on silicon layer 1, and a memory cell 11 is formed on the substrate 3 (Tanaka at Figure 1(f)). However, the silicon layer 1 is formed above the silicon substrate 3, which is completely different from the claimed invention. Thus, nowhere does Tanaka teach or suggest a first isolation oxide formed adjacent to a first end portion of the insulator layer, a second isolation oxide formed adjacent to a second end portion of the insulator layer and a third isolation oxide formed on a middle portion of the insulator layer, the first and second isolation oxides extending laterally beyond the first and second end portions, respectively. Therefore, Tanaka does not make up for the deficiencies of Sun.

Therefore, Appellant submits that these references would not have been combined and

even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

Further, Appellant submits that while independent claims 29, 41 and 45-46 are directed to statutory subject matter, as discussed above, claims 37-39 and 43-44 which each depend from one of claims 29 and 41, define similar statutory subject matter separately and distinctly from the independent claims as these dependent claims recite additional elements clearly providing useful, concrete and tangible results.

Specifically, Claim 36 depends from claim 29, and recites "*wherein a sidewall of said insulator layer is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer*"(Application at page 8, lines 17-21).

Claim 37 depends from claim 29, and recites "*further comprising: a memory device formed in said bulk silicon region; and a logic device formed in said SOI region*"(Application at page 15, lines 20-24).

Claim 38 depends from claim 37, and recites "*wherein said memory device comprises at least one of a dynamic random access memory (DRAM) device, a memory array, a static random access memory (SRAM) device, a flash memory device, a high voltage, high power circuit, and an analog circuit*"(Application at page 15, lines 20-24).

Claim 39 depends from claim 37, and recites "*wherein said logic device comprises at least one of a logic circuit, a P-FET device, an N-FET device, a low voltage, low power circuit, and a high performance digital circuit*"(Application at page 14, lines 16-21).

Claim 43 depends from claim 42, and recites "*wherein said substrate is part of a*

semiconductor device comprising a logic device formed in said silicon-on-insulator (SOI) region"(Application at page 6, line 17-page 16, line 5).

Claim 44 depends from claim 42, and recites "*wherein said substrate is part of a semiconductor device comprising a memory device formed in said bulk silicon region*"(Application at page 15, lines 20-24).

Therefore, the dependent claims 37-39 and 43-44 define elements and limitations which further place the claimed invention squarely in the realm of statutory subject matter and which provide a useful, tangible and concrete result.

Therefore, dependent claims 37-39 and 43-44, like independent claims 29, 41 and 45-46, include at least one element which is not taught or suggested by the cited references, or any combination of the cited references.

IX. CONCLUSION

In view of the foregoing, Appellant submits that claims 29-39 and 41-57, all the claims presently pending in the application, are patentably distinct from the prior art of record and in condition for allowance. Thus, the Board is respectfully requested to remove the rejections of claims 29-39 and 41-57.

Please charge any deficiencies and/or credit any overpayments necessary to enter this paper to Assignee's Deposit Account number 50-0510.

Respectfully submitted,

Dated: 4/19/04

Phillip E. Miller
Reg. No. 46,060

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, Virginia 22182-4100
(703)761-4100
Customer Number: 21254

Attachment: Appendix

APPENDIX

1-28. (Canceled)

29. A semiconductor device comprising:

a bulk silicon region comprising single crystal silicon; and

a silicon-on-insulator (SOI) region comprising:

an insulator layer which is formed beneath an upper portion of said single crystal silicon and has at least one lateral end portion adjacent to a lower portion of said single crystal silicon; and

at least one isolation oxide formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer,

wherein said at least one isolation oxide comprises a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first and second end portions, respectively.

30. The semiconductor device according to claim 29, wherein said at least one island of single crystal silicon comprises a plurality of islands and said at least one isolation oxide

comprises a plurality of isolation oxides, and each of said islands are interspaced between said isolation oxides to form a shallow trench isolation (STI) structure.

31. The semiconductor device according to claim 30, wherein said insulator layer has a thickness in a range of 1000Å and 5000Å.

32. The semiconductor device according to claim 29, wherein said upper portion of said single crystal silicon is formed over said insulator layer by depositing amorphous silicon on said insulator layer and said lower portion of said single crystal silicon, and crystallizing said amorphous silicon by using said lower portion of said single crystal silicon as a crystal growth seed.

33. The semiconductor device according to claim 32, wherein said isolation oxides are formed in defective portions of said single crystal silicon.

34. The semiconductor device according to claim 31, wherein said isolation oxides and said insulator layer are formed of a same material.

35. The semiconductor device according to claim 29, wherein an upper surface of said isolation oxides and said single crystal silicon are planarized.

36. The semiconductor device according to claim 29, wherein a sidewall of said insulator layer is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer.

37. The semiconductor device according to claim 29, further comprising:

a memory device formed in said bulk silicon region; and

a logic device formed in said SOI region.

38. The semiconductor device according to claim 37, wherein said memory device comprises at least one of a dynamic random access memory (DRAM) device, a memory array, a static random access memory (SRAM) device, a flash memory device, a high voltage, high power circuit, and an analog circuit.

39. The semiconductor device according to claim 37, wherein said logic device comprises at least one of a logic circuit, a P-FET device, an N-FET device, a low voltage, low power circuit, and a high performance digital circuit.

40. (Canceled)

41. A hybrid bulk silicon and silicon-on-insulator (SOI) substrate, comprising:

an insulator layer which is formed beneath an upper portion of single crystal silicon and

on a lower portion of said single crystal silicon; and

a plurality of isolation oxides formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer,

wherein said plurality of isolation oxides comprises a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first and second end portions, respectively.

42. The hybrid substrate according to claim 41, wherein said insulator layer is formed in an SOI region of said substrate and not in a bulk silicon region of said substrate.

43. The hybrid substrate according to claim 42, wherein said substrate is part of a semiconductor device comprising a logic device formed in said silicon-on-insulator (SOI) region.

44. The hybrid substrate according to claim 42, wherein said substrate is part of a semiconductor device comprising a memory device formed in said bulk silicon region.

45. A semiconductor device comprising:

a bulk semiconductor region comprising semiconductor substrate; and

a semiconductor-on-insulator region comprising:

an insulator layer which is formed beneath an upper portion of said semiconductor substrate and has at least one lateral end portion adjacent to a lower portion of said semiconductor substrate; and

at least one isolation oxide formed in said upper portion of said semiconductor substrate so as to form at least one island of said semiconductor substrate on an upper surface of said insulator layer,

wherein said at least one isolation oxide comprises a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first and second end portions, respectively.

46. A semiconductor device comprising:

a single crystal silicon substrate having a lower portion and an upper portion;

an insulator layer which is formed beneath said upper portion of said single crystal silicon substrate and on said lower portion of said single crystal silicon substrate; and

at least one isolation oxide formed in said upper portion of said single crystal silicon substrate so as to form at least one island of said single crystal silicon substrate on an upper surface of said insulator layer,

wherein said at least one isolation oxide comprises a first isolation oxide formed adjacent

to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first and second end portions, respectively.

47. The semiconductor device according to claim 46, wherein said upper portion of said single crystal silicon substrate is formed on said insulator layer by growing said single crystal silicon substrate horizontally over said insulator layer.

48. The semiconductor device according to claim 46, wherein said upper portion of said single crystal silicon is formed by depositing amorphous silicon on said insulator layer and said lower portion of said single crystal silicon substrate, annealing said amorphous silicon so that, using said lower portion of said single crystal silicon substrate as a crystal growth seed, said amorphous silicon is converted to single crystal silicon having a same orientation as said lower portion of said single crystal silicon substrate.

49. The semiconductor device according to claim 48, wherein said isolation oxides are formed by forming isolation trenches in defective portions of said upper portion of said single crystal silicon, and depositing oxide in said isolation trenches.

50. The semiconductor device according to claim 29, wherein an angle between a bottom

surface of said insulator layer and a sidewall of said insulator layer is about 103°.

51. The semiconductor device according to claim 29, wherein a crystal orientation and structure of said upper portion of said single crystal silicon follows a crystal orientation and structure of said lower portion of said single crystal silicon.

52. The semiconductor device according to claim 29, wherein said upper portion of said single crystal silicon comprises crystallized amorphous silicon.

53. The semiconductor device according to claim 29, wherein said insulator layer has a width in a range of about 2 μm to 10 μm.

54. The semiconductor device according to claim 29, wherein said upper portion of said single crystal silicon has a thickness in a range of about 500 Å to 3000 Å.

55. The semiconductor device according to claim 30, wherein said plurality of islands of single crystal silicon are wholly formed on said insulator layer.

56. The semiconductor device according to claim 29, wherein said at least one island of single silicon crystal is substantially devoid of a defective region.

57. The semiconductor device according to claim 29, wherein said first and second isolation oxides are formed at least partially on said first and second end portions, respectively.